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10/648,181	08/26/2003	Satoki Shibayama	0828.68273	4420

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,181	SHIBAYAMA ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 -14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/26/03 and 1/6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 14 are pending.

Claim Rejections - 35 USC § 112

2. Claims 7 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7 and 12 recite the limitation "the processors are distributed over a plurality of nodes" which is considered unclear. Examiner is not clear how processor (hardware) can be distributed over the network. Furthermore, examiner is unable to find any support in applicant's specification for such disclosure. Examiner believes this might be a typographical error. For the purpose of the examination, the examiner will assume applicant means "the processes are distributed over a plurality of nodes" instead. Clarification is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention.was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 3, 8, 9, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Koeda "Operating System of the VX/VPP300/VPP700 Series of Vector-Parallel Supercomputer Systems", Applicant's submitted IDS filed 8/26/03 (hereinafter Koeda).

5. Regarding **claim 1**, Koeda discloses a parallel process execution method with which a plurality of processors execute a plurality of parallel processes produced from a parallel program together with other processes in a time-shared fashion, the method comprising the steps of (page 19 fig. 2):

a) setting a time allocation ratio that determines how much of a given cycle period should be allocated for execution of the parallel program (page 20 fig 3, page 19 left col. paragraph 1 – 2);

b) assigning each parallel process of the parallel program to one of the plurality of processors, and starting execution of the assigned parallel processes simultaneously on the plurality of processors(page 19 left col. paragraph 1 – right col. paragraph 2); and

c) stopping the execution of the assigned parallel processes simultaneously on the plurality of processors, when the time elapsed since the start of the parallel processes has reached a point that corresponds to the time allocation ratio that has been set to the parallel program (page 19 left col. paragraph 2 – right col. paragraph 2).

6. Regarding **claim 2**, Koeda discloses the parallel process execution method according to claim 1, wherein said setting step a) sets the time allocation ratio to the parallel program by

dividing the given cycle period into a plurality of time slots and determining which process to execute in each time slot of the different processors (page 20 fig. 3)

7. Regarding **claim 3**, Koeda discloses the parallel process execution method according to claim 2, wherein the processes to be executed in the time slots include interactive processes (page 20 fig. 3).

8. **Claims 8, 9, 13 and 14** are rejected on the same grounds as stated in claims 1- 2 above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4 – 7 and 10 - 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koeda, "Operating System of the VX/VPP300/VPP700 Series of Vector-Parallel Supercomputer Systems".

11. Regarding **claim 4**, Koeda discloses that PE allocation according to job class (page 18 right col. paragraph 8) and that if there is an idle part of a PE, the submitted job are sequentially allocated to the PE and executed in Shared mode which share the same PE (page 20 left col. paragraph 2). Therefore, it would have been obvious for one of an ordinary skill in the art at the

time the invention was made to recognize that Koeda's disclosure suggests the steps of providing a set of criteria beforehand for use in determining what to execute in a free time slot that has no process assigned and according to the criteria, selecting at each of the processors which process to be executed in the free time slot because part of Koeda's invention is about resource assignment and scheduling in which jobs must be scheduled to use the parallel processing system effectively (page 18 right col. paragraph 6).

12. Regarding **claim 5**, Koeda discloses the parallel according to claim 4, wherein:

the criteria include process execution method a throughput-first policy which allows batch processes to run in the free time slot, and a turnaround-first policy which allows no batch process to run in the free time slot (page 18 right col. paragraph 8: PE allocation according to job class. Page 19: left col. paragraph 2 - 3: The cpu distribution ratio can be set for the scheduling class for interactive processing and the scheduling class for batch processing); and

said selecting step selects either the throughput-first policy or the turnaround-first policy (page 20 left col. paragraph 2: If there is an idle part of a PE, the submitted job are sequentially allocated to the PE and executed in Shared mode).

13. Regarding **claim 6**, Koeda discloses the parallel process execution method according to claim 5, wherein the throughput-first policy gives successively lower priorities to interactive processes, non-parallel processes for execution on a single processor, and parallel processes (page 18 left col. paragraph 3: in a PE for interactive processing only, execution of batch job is

suppressed. Page 9 right col. paragraph 4: in resource allocation, jobs with a higher memory priority are the first jobs to acquire resources).

14. Regarding **claim 7**, Koeda discloses the parallel process execution method according to claim 1, wherein the processors are distributed over a plurality of nodes (fig. 2), and the method further comprises the steps of:

causing simultaneous interrupts to the nodes (page 20 right col. paragraph 5: urgent job can be executed earlier than other jobs by submitting the urgent job to the queue. Fig. 5);

sending the received interrupts simultaneously to every processor in the nodes (fig. 5); and

causing the processors to start the cycle period in phase with the interrupts (fig. 5).

15. **Claims 10 – 12** are rejected on the same grounds as stated in claims 1, 4, 5 and 7 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lilian Vo
Examiner
Art Unit 2195

lv
June 20, 2007

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